WHAT IS CLAIMED IS:

1. A chip-stacked package comprising:

a doubly down-set leadframe having a down-set tip to be wire-bonded;

a first semiconductor chip attached under the down-set tip of the leadframe;

a first metal wire electrically connecting bonding pads of the first semiconductor chip with the down-set tip of the leadframe;

a second semiconductor chip attached on the leadframe;

a second metal wire electrically connecting the second semiconductor chip with the leadframe; and

an epoxy molding compound encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the leadframe while exposing the backside of the first semiconductor chip.

2. The chip-stacked package of Claim 1, wherein the first semiconductor chip is attached by means of an LOC tape.

3. The chip-stacked package of Claim 1, wherein the second semiconductor chip is attached by means of adhesives.

4. The chip-stacked package of Claim 3, wherein the adhesives are filled in the entire space between the second semiconductor chip and the first semiconductor chip.

5. The chip-stacked package of Claim 3, wherein the adhesives are interposed only between the second semiconductor chip and the leadframe.

6. The chip-stacked package of Claim 1, wherein the second semiconductor chip is attached by means of an adhesive tape.

7. A chip-stacked package comprising:

a doubly down-set leadframe having a down-set tip to be wire-bonded;

a first semiconductor chip attached under the leadframe by means of a B-stage material;

a first metal wire electrically connecting bonding pads of the first semiconductor chip with the tip of the leadframe;

a second semiconductor chip attached on the leadframe by means of adhesives;

a second metal wire electrically connecting the second semiconductor chip with the leadframe; and

an epoxy molding compound encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the leadframe while exposing the backside of the first semiconductor chip.

8. A chip-stacked package comprising:

a down-set leadframe having a tip to be wire-bonded, the tip being designed in such a manner as to have a relatively small thickness;

a first semiconductor chip attached under the tip of the leadframe;

a first metal wire electrically connecting bonding pads of the first semiconductor chip with the tip of the leadframe;

a second semiconductor chip attached on the leadframe;

a second metal wire electrically connecting the second semiconductor chip with the leadframe; and

an epoxy molding compound encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the leadframe while exposing the backside of the first semiconductor chip.